

Multi-Wafer Surface Ion Traps: Enhanced Trap Depth, Vertical Confinement, and Ion Lifetime Through Increased Wafer Separation

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ABSTRACT

Surface ion traps are a cornerstone technology for scalable quantum information processing, yet their shallow trap depths and limited ion lifetimes remain fundamental engineering bottlenecks. This study presents a systematic experimental and statistical comparison between standard single-wafer surface traps and a novel multi-wafer surface trap architecture in which two parallel wafers with integrated radio-frequency (RF) electrodes are separated by a controllable vertical gap. Seventeen trap configurations were characterized ($N = 5$ standard, $N = 12$ multi-wafer), with wafer separations ranging from 50 to 500 μm . Welch's independent-samples t-tests revealed that the multi-wafer geometry produced a mean trap depth of 23.53 meV compared with 8.50 meV in standard traps ($d = 2.71$, $p < .001$), extended ion lifetimes from 120 s to 620.75 s ($d = 2.72$, $p < .001$), and reduced anomalous heating rates from 857 to 153 quanta/s ($d = -14.75$, $p < .001$). Pearson correlations showed an exceptionally strong positive relationship between wafer separation and trap depth ($r = .999$, $p < .001$), and between trap depth and ion lifetime ($r = .997$, $p < .001$). A linear regression model explained 99.4% of the variance in ion lifetime from trap depth alone ($R^2 = .995$). Qubit coherence time (T_2^*) scaled with trap depth, reaching 18.2 ms in the deepest configuration. Results demonstrate that multi-wafer architectures overcome the characteristic depth saturation (~ 5.5 meV) of standard designs and produce deeper, more stable, and longer-lived ion traps suitable for scalable quantum computing.

Keywords: *surface ion trap, multi-wafer architecture, trap depth, ion lifetime, quantum computing, anomalous heating, vertical confinement*

Introduction

Trapped-Ion Quantum Computing: Promise and Engineering Challenges

One of the most important ambitions of the physics and engineering of the modern era is the realization of large-scale quantum computers with the ability to implement algorithms that are out of reach of classical hardware. Among the numerous systems with this aim, such as superconducting qubits, photonic systems, and neutral atoms, trapped ions have become one of the most promising systems due to their very high quality qubits. Trapped-ion systems have established performance metrics such as long coherence times, nearly unity single-qubit gate fidelities, and inherent all-to-all qubit connectivity within a single trapping volume that serve as a benchmark against which other architectures are often compared (Bruzewicz et al., 2019; Moses et al., 2023). In early experiments, macroscopic three dimensional Paul traps were used to confine ions, with deep pseudopotential wells, in the range of one to a few electron volts, to assure strong trapping, long ion life and insensitivity to background-gas collisions and variations of an external electric field.

Nevertheless, although these physical benefits exist, a realistic implementation of a fault-tolerant quantum processor would need thousands or millions of qubits, and it is impractical to maintain such a large number of qubits in one trapping zone of a typical macroscopic system. The scalability issue has motivated the area to miniaturized, microfabricated trap designs. The first surface ion traps, in which all the electrodes are on a single planar surface and the ion cloud is suspended over the chip surface, were demonstrated in the mid-2000s (Seidelin et al., 2006; Stick et al., 2006) and quickly became popular since they can be produced via conventional semiconductor photolithography. This is compatible with microfabrication infrastructure, which enabled the inclusion of on-chip waveguides, microwave delivery circuits, photodetectors, and multi-zone shuttling designs that will be needed to develop a modular quantum computing roadmap (Romaszko et al., 2020; Mehta et al., 2020).

But there was a trade-off inherent to the switch to macroscopic to planar surface geometry: a very huge reduction in trap depth. Macroscopic traps are regularly made to reach depths of hundreds of megahertz (megaelectron volts (meV)) to

electron volts, whereas single-wafer surface traps are limited by geometry to depths around 5 to 8 meV. This superficial constraint is not due to inadequate radio-frequency (RF) drive voltage but a geometrical constraint of the one-sided planar electrode layout, whose analysis is formally based on the Earnshaw theorem (Wesenberg, 2008). The axial trapping frequency increases with increasing drive voltages, at the cost of the pseudopotential barrier, the effective height of the trapping potential well, which saturates at around 5.5 meV and cannot be further raised with further drive voltages, without changing the geometry of the electrodes themselves (Allcock et al., 2012; Chiaverini et al., 2005). This saturation is among the most important engineering bottlenecks that face surface-trap-based quantum processors and drives the innovation in architecture discussed in the current study.

Anomalous Heating: The Second Fundamental Bottleneck

Intimately connected with the trap-depth problem is the effect of anomalous motional heating- an overexcitation of the vibrational modes of the trapped ion by many orders of magnitude more than would be possible due to thermal Johnson-Nyquist noise of the electrode resistances. Anomalous heating has been comprehensively reviewed with fluctuating patch potentials and thermally activated surface adsorbates being the most likely physical processes, with the rate of heating ($\dot{n}$) varying as $(d)^{-4}$ as ion-electrode distance (d) and $1/B^2$ of the square of the trap secular frequency (Brownnutt et al., 2015; Sedlacek et al., 201). Even in standard surface traps, in which ions are suspended only 50-100 μ m above the electrode plane, anomalous heating rates of hundreds and even thousands of motional quanta per second are commonly observed at room temperature and can continue to be observed at high rates even at cryogenic temperatures.

Anomalous heating is not just a nuisance that decreases the coherence times; it directly determines two-qubit gate fidelity - the most operationally significant figure of merit of a quantum processor. The entangling power of the qubit states in the scheme of the Mollmer-Sorensen interaction and other geometric-phase schemes lies in the fact that the qubit states are entangled by the interaction of the qubits via common motional modes. Overoccupation of phonons when executing a gate creates phase errors, which increase exponentially, and restrict the fidelity ceiling of a

particular experimental platform (Bruzewicz et al., 2019). As a result, any architectural change that raises the separation between the ion-electrode, and thus decreases the anomalous heating rate, can be directly translated into better gate fidelity, and a corresponding reduction in overhead of quantum error correction. The long-standing (d) -4 dependence causes even moderate changes in ion height to be very effective: a doubling of the ion-electrode distance causes the heating rate to decrease sixteen-fold.

The planar traps have the anomalous heating problem compounded by surface dielectric charging. Since laser beams required to cool, prepare states and read out inevitably strike the electrode surface or surrounding dielectrics, they cause photoelectron emission and the slow development of patches of stray charge that drift the RF null position, cause additional micromotion, and distort the axial potential landscape (Harlander et al., 2010; Berkeland et al., 1998). The standard countermeasuring, micromotion compensation, involves a real-time adjustment of DC compensation voltages, and has a calibration overhead that increases with the number of ions. The multi-wafer architecture has a structural mitigation mechanism to both anomalous heating and micromotion susceptibility by virtue of its symmetric vertical geometry which decouples the ion position with single-side stray field perturbations, and a structural mitigation mechanism to both anomalous heating and micromotion susceptibility.

Multi-wafer surface ion traps are designed to overcome the geometric limitations of planar traps by having two electrode bearing wafers in a face-to-face geometry, separated by a tightly spaced vertical gap. In the simplest implementation, RF electrodes are patterned on both wafers, and driven with the correct phase relationships to create a pseudopotential null floating between the surfaces. The geometry is conceptually similar to a linear Paul trap, using four rod electrodes but has the planar lithographic geometry enabling microfabrication (Hughes et al., 2011; Stick et al., 2006). The composite pseudopotential due to an ion at the midpoint has the advantage of having both planes of electrodes contribute to its depths, giving rise to depths that in theory depend nearly linearly on the distance between the wafer-to-wafer, but goes into a saturation regime as the ion-electrode distance

approaches the distance between the wafer-to-wafer.

Analytical expressions of the electrostatics of surface-electrode ion traps formed the theoretical basis of multi-wafer trapping by Wesenberg (2008) who demonstrated that dual-plane geometries radically change the depth-voltage relationship compared to single-sided ion traps. Schmied et al. (2009) performed numerical simulations to extrapolate these predictions down to realistic geometries of electrodes and confirmed that it was possible to achieve trap depths of 1530 meV and even higher at separations of 200500 μm with drive parameters available with standard electronics. These theoretical expectations were generally in line with the initial experimental observations of multi-wafer traps (Maunz, 2016) that claimed trap depths of between 15 and 30 meV and ion lifetimes of more than 10 minutes- an order of magnitude longer than single-wafer surface traps at similar vacuum pressures.

These initial results have been verified and generalized by more recent experimental realizations. Clark et al. (2021) showed high-fidelity Bell-state preparation in a multi-wafer trap system, making use of the longer coherence time made possible by the deeper potential and the low heating. Similar advances in integrated photonics have demonstrated that multi-wafer designs have geometrical benefits in routing optical fibers and waveguides between the two electrode planes, enabling the implementation of integrated optical addressing schemes (Mehta et al., 2020). The multi-wafer paradigm was singled out by the Romaszko et al. (2020) review of microfabricated ion traps as one of the most promising near-term directions of extending the performance envelope of surface-trap-based processors, mentioning the capability to independently optimize the upper and lower electrode planes to serve various functional purposes, such as RF confinement, DC shuttling control, integrated optics

Although this evidence has been growing, one important gap has been in the literature: there has been no systematic, multi-parameter characterization of performance metrics (trap depth, ion lifetime, anomalous heating rate, vertical confinement profile and qubit coherence time) as a continuous function of wafer separation in both the standard and multi-wafer trap families. Most published works

have studied a single trap geometry, or a limited number of operating points, which is challenging to scale to extract scaling laws or determine the design regimes to achieve the most performance with particular quantum computing applications. The current study was specifically aimed to fill this gap.

Ion Lifetime and Its Operational Significance

An important operation measure of any quantum processor is ion lifetime, which is the average time between ion loading and ion loss, which restricts the maximum number of steps a circuit can execute before the computation is interrupted by a reloading process. In a multi-ion processor with fault tolerance algorithm, the loss of ions in one zone results in an expensive recovery process: the zone needs to be reloaded, the ion needs to be sympathetically cooled and re-initialized and the entangled state of the ions in adjacent zones will frequently need to be checked and re-checked. These overheads scaled by the number of qubits and longer computations mean that ion lifetime demands at the system level (Pagano et al., 2019; Moses et al., 2023).

Background-gas molecules collisions with the ion loss in surface traps are dominated by the background-gas molecules, in ultra-high vacuum (UHV) systems, which consist of hydrogen and helium, which provide enough kinetic energy to overcome the pseudopotential barrier. The loss per collision probability is proportional to trap depth, hence, a deeper trap would need a higher collision energy to eject the ion and the distribution of collision energy in a thermal distribution, hence, the loss rate decreases exponentially with trap depth. Experimental measurements of several groups suggest that lifetimes of typical surface traps in pressures of 0.10 -0.19 Pa are between 60 and 180 seconds (Pagano et al., 2019), which are at the shallow trapping depths of the single-wafer design. Background-gas partial pressures can be reduced by another few orders of magnitude by cryogenic operation, but requires large cryogenic infrastructure, which can greatly extend lifetimes (Pagano et al., 2019). Another way forward is multi-wafer traps: by increasing the depth of the pseudopotential potential well at room temperature or relatively low cryogenic temperatures, they can obtain lifetime enhancements as good as those achieved by simply cryogenic suppression of background gas.

Theoretical expectation of the relationship between the trap depth and the ion lifetime is that it should be monotonically increasing, but may not be linear, as the background-gas collision cross-section and the energy-transfer processes add other dependencies to the relationship between secular frequency and mass. Both a useful practical engineering design tool and a primal test of ion-loss models have been empirically characterised through much of this relationship, over a large range of trap depths—including both standard and multi-wafer designs in a single internally consistent experimental campaign. The extremely strong Pearson correlation ($r = .997$) and the almost perfect linear regression fit ($R^2 = .995$) that the present study reports are the most statistically rigorous evidence to date that this relationship does exist over such a large parameter space.

In addition to ion lifetime, the most direct predictor of the gate fidelity is the qubit dephasing time T_2 , which is limited by various dephasing mechanisms: magnetic-field fluctuations that cause a change in the qubit transition frequency, anomalous motional heating that introduces phase diffusion in the qubit due to the interaction between the spin and the motion, and trap-frequency instability due to drift in the stray- The latter two channels and decreasing the T_2 that can be attained in the absence of active field stabilization are more sensitive to perturbations of stray DC fields in shallower traps, making the former more sensitive to such perturbations.

Multi-wafer metals are predicted to enhance T_2 by at least three mechanisms which are coupled. The deeper pseudopotential is first based on more solid confinement, which makes the equilibrium position of the ion less prone to shifts due to the stray fields. Second, the lower anomalous heating rate, proportional to ion-electrode distance (d^{-4}), reduces the motional dephasing rate and provides ground-state cooling protocols with increased opportunities to keep phonon occupancies low (Turchette et al., 2000). Third, the balance between the stray fields of the two electrode planes in the multi-wafer geometry is a symmetric vertical geometry, which offers a more stable null position, which is less susceptible by nature to the occurrences of differential charging. These mechanisms together are predicted to result in a coherence time which depends on trap depth, and the current study is the

first systematic experimental proof of this dependence over seventeen trap designs of both single and multi-wafer designs.

The usefulness of the enhanced T₂ is beyond measure. The fault-tolerant quantum computation threshold theorem states that the physical error rate per gate must be below a critical threshold - usually expected to be on the order of 1% in the surface code - which directly depends on the ratio between the gate time and the coherence time (Bruzewicz et al., 2019). Molmer-Sorensen gates Two-qubit Moldmer-Sorensen gates in trapped ions systems now take times of around 0.1-1 ms; tens of milliseconds coherence times are thus needed to get error rates which are uniformly below threshold. This threshold requirement is directly linked to the coherence time of 18.2 ms obtained with the deepest multi-wafer configuration of the present work (MW_500_OPT) which means that the multi-wafer platform is capable of fault-tolerant operation of the gate with current laser stability issues.

Scalable processor experiments like the race-track trapped-ion quantum processor in Moses et al. (2023) and the trapped-ion quantum CCD architecture in Pino et al. (2021) have shown that the ion lifetime, coherence time, and gate fidelity need to be collectively optimized at a system level. The propagation of individual changes in any single parameter through the error budget is complex, and the capability to optimize trap depth, ion lifetime, coherence time and heating rate simultaneously, as the current study shows, is possible in the multi-wafer geometry, qualitatively superior to a single-parameter optimization strategies.

Rationale, Research Objectives, and Hypotheses

In the light of the above theoretical predictions and existing body of evidence in the literature on the topic, the overall motivation behind the current study was to present a complete statistically rigorous comparison of standard and multi-wafer surface ion traps over a systematically varied design space. Previous work, though very informative, usually only described one or two trap geometries, and a limited number of performance indices, and it was hard to derive continuous scaling laws, or to determine which combination of design parameters optimized overall quantum-computing performance. This gap was filled in the present study, which produced and characterized seventeen different trap configurations (5 standard single-wafer

traps and 12 multi-wafer traps with wafer separations between 50 and 500 μm and determined the trap depth, ion lifetime, anomalous heating rate, vertical confinement profile, motional frequency, and qubit coherence time of each trap under strictly controlled experimental conditions.

Welch independent-samples t-tests between-group tests were used to statistically analyze the data as the framework of statistical analysis, Pearson product-moment correlations to describe the scaling relationships, and simple linear regression to characterize the predictive modeling of the ion lifetime as a trap depth function. The rationale behind Welch using a correction was that the two trap families have significant differences in terms of sample size and within-group variance, a condition where the standard Student t-test has an inflated Type I error rates (Delacre et al., 2017). Cohen d was reported with traditional significance levels of 0.2, 0.5, and 0.8 indicating small, medium, and large effects (Cohen, 1988) which offered a scale-free measure of practical significance that supplements the inferential p-values.

The experiment had four main hypotheses: (a) that the trap depth should increase monotonically and significantly with the separation between the wafers in multi-wafer designs, above the geometric saturation ceiling of standard traps; (b) that the ion lifetime is directly proportional to trap depth in both trap families, with a regression slope and coefficient of determination large enough to permit predict

The rest of this paper is structured in the following way. The Method section includes the trap designs and fabrication process, the experimental apparatus and the vacuum system and the laser systems, the protocols of measurement of each performance metric, and the procedures of statistical analysis. The Results section includes descriptive statistics, between-group inferential statistics, Pearson correlations, the linear regression model, and the comprehensive characterization of the wafer-separation to trap-depth scaling law and its downstream implications on the ion lifetime, heating rate, vertical confinement, and coherence time. These findings are discussed in the context of previous theoretical and experimental literature in the Discussion section, which evaluates the practical implications of the study to develop scalable quantum-computing hardware design, recognizes the

limitations of the study, and presents future research directions. The Conclusion draws a conclusion on the main findings and their implications to the field.

Multi-Wafer Surface Ion Traps: Enhanced Trap Depth, Vertical Confinement, and Ion Lifetime Through Increased Wafer Separation

Scalable quantum information processing has been proposed to be executed on trapped-ion quantum computing due to its long coherence times, high single and two-qubit gate fidelities as well as inherent all-to-all qubit connectivity in a single trap zone (Bruzewicz et al., 2019; Moses et al., 2023). However, the shift towards planar surface traps, with two-dimensional geometries that can be fabricated by standard semiconductor fabrication techniques, has increasingly become the focus of the field since initial demonstrations of planar surface-based traps in the early 2000s (Seidelin et al., 2006), and thus allows integrated optics, on-chip waveguides, and multi-zone ion shuttles. Although surface traps have these benefits, they have two interconnected and well-known drawbacks: small trap depths and uncharacteristically large motional heating rates due to noise in electric fields at the electrode surfaces (Brownnutt et al., 2015; Sedlacek et al., 2018).

The height of the pseudopotential barrier that traps the ion, known as trap depth, dictates directly the ion lifetime, ability to withstand collisions with background gas, and the useful space of voltage-frequency parameter space accessible to experimentalists. To achieve high saturation rates of the standard surface traps made out of single wafers, the trap depths of around 5 to 8 meV are usually saturated even with increased radio-frequency (RF) drive voltages (Allcock et al., 2012; Chiaverini et al., 2005) due to the planar geometry of electrodes on the chip surface, where trapping nulls occur only. This is a direct consequence of the Earnshaw theorem applied to the planar electrode which is a single-sided: as the RF voltage is increased, the trap frequency increases, but it makes only a small contribution to the escape barrier (Wesenberg, 2008). Consequently, the ion loss rates in the typical surface traps are still dominated by background-gas interactions, and the reported lifetimes are generally between 1 and 3 min at ultra-high vacuum (Pagano et al., 2019).

Multi-wafer surface trap architecture is used to solve this geometric constraint with

two RF carrying wafers in parallel with each other, separated by a controlled vertical cavity (usually 100 to 500 000 m). The resulting geometry of four rods is a composite of the manufacturability of planar lithography and deep pseudopotential of three-dimensional traps (Hughes et al., 2011; Stick et al., 2006). Theoretical studies of Wesenberg (2008) and numerical simulations by Schmied et al. (2009) had predicted that the depth of the traps of such geometries of dual-wafer should increase approximately linearly with wafer separation at moderate separations, and then eventually enter a saturation regime as the ion-electrode separation approaches the inter-wafer separation. Recent experimental realizations have started to confirm these predictions, with trap depths of between 15 and 30 meV and ion lifetimes of over 10 min (Clark et al., 2021; Maunz, 2016).

In addition to the trap depth, the multi-wafer geometry also perturbs the spatial profile of the pseudopotential in scalable quantum computing-relevant ways. Since the RF null is now floating between two grounded or counter-driven planes, the vertical confinement is wider and more balanced, and eliminates the sensitivity of the ion position to stray static fields and anomalous charging of the surface (Berkeland et al., 1998; Harlander et al., 2010). Moreover, the anomalous heating is directly suppressed due to the increased ion-electrode distance that can be reached in multi-wafer designs that empirically depends on d as d (Brownutt et al., 2015; Sedlacek et al., 2018). Reduced heating rates correspond to an increase in motional coherence times, and eventually lead to an increase in the two-qubit gate fidelities.

Although the theoretical attractiveness of multi-wafer architectures and the increasing body of experimental evidence has been pivotal, quantitative comparisons between standard and multi-wafer traps, especially those that characterize trap depth, vertical confinement, ion lifetime, heating rate, and qubit coherence all as a function of wafer separation have been relatively scarce. Published reports typically have studied one trap geometry or a small set of parameters, and it is not easy to find general scaling laws or determine the design regimes that are optimal quantum computing applications.

The current research tackles this knowledge gap by presenting a systematic description of 17 trap configurations with a large diversity of wafer separations (50

to 500 μm) and drive conditions. The four main hypotheses we test are: (a) the depth of a trap monotonically and substantially increases with the distance between wafers in multi-wafer designs and (b) the ion lifetime is linear with the depth of a trap across both trap families; (c) the anomalous heating rate is proportional to trap depth, associated with a corresponding increase in the ion-electrode distance; and (d) the qubit coherence. We test all these hypotheses with the help of descriptive statistics, Welch independent-samples t-tests, which is strong in the face of unequal sample sizes and variances (Delacre et al., 2017), Pearson correlations, and linear regressions.

Method

Trap Design and Fabrication

There were two types of surface ion traps studied. ST The standard surface trap (ST) set-up involved a single silicon wafer, with microfabricated gold-on-silicon-dioxide electrodes, created through standard photolithography and electron-beam evaporation. The ion-electrode separation was about 70 μm and three different variants (Std_50um, Std_100um, Std_150um) varied with varying central electrode width. The multi-wafer (MW) surface trap was a two-wafers (one RF and one DC) surface trap with identically-patterned electrodes on both surfaces mounted in a precision machined titanium frame with a manageable vertical gap between 200 and 500 μm . Parallelism of the wafer was checked using the optical probe to a tolerance of 10 mm active area of the wafer with a range of $\pm 2 \mu\text{m}$. There were seven main MW structures (MW 200um to MW 500um) with two high-drive optimized designs (MW 500 HV and MW 500 OPT) to test the maximum limit of trap depth possible.

Experimental Apparatus

Calcium-40 ions ($^{40}\text{Ca}^+$) were loaded into each trap via isotope-selective photoionization. Experiments were carried out in a cryogenic ultra-high vacuum chamber at background pressures of 1.0×10^{-9} and 1.4×10^{-9} Pa, as measured, per configuration. RF drive frequencies were between 10 and 16 MHz and RF voltages were between 85 and 185 V peak and tuned to give the best trap depth and constant confinement (q-parameter < 0.4). The cooling of the $4\text{S}_{1/2} \leftrightarrow 4\text{P}_{1/2}$ transition at 397 nm was done using Doppler cooling, and the repumping at 866 nm

in the $3D_{3/2} \leftrightarrow 4P_{1/2}$ manifold. A photomultiplier tube and an electron-multiplying CCD camera detected ion fluorescence, which is in line with standard protocols (Leibfried et al., 2003; Wineland et al., 1998).

Measurements

Trap Depth.

The depth of traps was calculated through the numerical integration of the pseudopotential with geometries of the electrodes measured and applied RF voltages in the Wesenberg (2008) method. In every configuration, the experimental depth was checked by measuring the minimum RF voltage needed to trap an ion in the presence of an axial perturbation of the electric-field with a controlled depth.

Ion Lifetime.

The ion lifetime was determined as the average survival of one Doppler-cooled ion between loading and loss events without any active perturbations. To each configuration, three to five independent loading cycles were measured (minimum five cycles to measure standard traps, variable to measure MW traps), and the arithmetic mean was taken as the reported lifetime. Sudden, sustained loss of fluorescence was used as a detection of loss events.

Heating Rate.

The rate of motional heating (in quanta per second, $\dot{n}$) was determined (Turchette et al., 2000) by determining the ratio of the red and blue sideband excitation probabilities following a controlled wait period.

Qubit Coherence.

The optical qubit dephasing time T_2^* was measured using Ramsey interferometry on the $4S_{1/2} \leftrightarrow 3D_{5/2}$ quadrupole transition (729 nm) with 5 to 10 measurements per configuration.

Statistical Analysis

Python 3.11 with SciPy (Virtanen et al., 2020) and Pingouin (Vallat, 2018) were used to conduct statistical analyses. The Welch independent-samples t-tests, which do not presuppose equal variances, were used to compare between groups of trap depth, ion lifetime, heating rate and motional frequency and are recommended in unequal sample sizes (Delacre et al., 2017). The effect sizes are given as Cohen d, with

traditional values of 0.2, 0.5, and 0.8 that indicate small, medium, and large effects (Cohen, 1988). Pearson product-moment correlation was calculated between the significant design and performance variables and the 95% confidence interval calculated using r-to-z transformation of Fisher. Simple linear regression model was used to model the relationship between trap depth and ion lifetime and the coefficient of determination (R^2), adjusted (R^2) and F- statistic were reported. Statistical significance was considered $\alpha = .05$ (two-tailed) and all confidence intervals are reported at 95% confidence.

Results

Descriptive Statistics

Table 1 presents descriptive statistics of all four main outcomes. Standard traps yielded a mean trap depth of 8.50 meV (SD = 0.16, N = 5) and a mean ion lifetime of 120.0 s (SD = 3.81). Multi-wafer traps produced substantially higher mean trap depths of 23.53 meV (SD = 7.84, N = 12) and ion lifetimes of 620.75 s (SD = 260.54). The scatter in the MW group is an intentional sweep on wafer separation between 200 and 500 μm , but the standard traps were reenacted at one design point. The mean rate of anomalous heating (in quanta/s) of the standard group was 857.0 and of the MW group was 153.25, which is a reduction of about 82 percent.

Table 1 Descriptive Statistics by Trap Type

Group	Variable	N	M	SD	SE	Min	Mdn	Max
Standard	Trap depth (meV)	5	8.50	0.16	0.07	8.30	8.50	8.70
Standard	Ion lifetime (s)	5	120.00	3.81	1.70	115.00	120.00	125.00
Standard	Heating rate (q/s)	5	857.00	23.35	10.44	830.00	850.00	890.00
Standard	Motional freq. (MHz)	5	1.20	0.00	0.00	1.20	1.20	1.20
Multi-wafer	Trap depth (meV)	12	23.53	7.84	2.26	15.70	23.40	35.90

Multi-wafer	Ion lifetime (s)	12	620.75	260.54	75.21	372.00	575.50	1065.00
Multi-wafer	Heating rate (q/s)	12	153.25	63.33	18.28	65.00	148.00	235.00
Multi-wafer	Motional freq. (MHz)	12	1.81	0.32	0.09	1.50	1.80	2.30

Note. M = mean; SD = standard deviation; SE = standard error of the mean; Mdn = median; q/s = motional quanta per second. Standard traps were measured at a fixed design point; multi-wafer traps span wafer separations of 200 to 500 μm .

Between-Group Differences

The independent-samples t-tests of Welch showed that all the four main outcomes were significantly different between the types of traps, and all the effect sizes were enormous (> 2.7 ; Cohen, 1988). Table 2 reports the entire results of the test. Trap depth was 15.03 meV greater in the MW group (95% CI $[-10.05, 20.02]$), $t(11.02) = 6.64$, $p < .001$, $d = 2.71$. Ion lifetime was extended by 500.75 s on average (95% CI $[-335.19, 666.31]$), $t(11.01) = 6.66$, $p < .001$, $d = 2.72$. Heating rate was reduced by 703.75 quanta/s (95% CI $[-748.63, -658.87]$), $t(14.97) = -33.43$, $p < .001$, $d = -14.75$, representing the largest effect size observed in the study. Motional frequency was also higher in the MW group by 0.61 MHz (95% CI $[0.41, 0.81]$), $t(11.00) = 6.58$, $p < .001$, $d = 2.69$.

Table 2: *Welch's Independent-Samples t-Tests Comparing Standard and Multi-Wafer Traps*

Variable	M (MW)	M (Std)	Diff.	t	df	p	d
Trap depth (meV)	23.53	8.50	15.03	6.64	11.02	$< .001$	2.71
Ion lifetime (s)	620.75	120.00	500.75	6.66	11.01	$< .001$	2.72
Heating rate (q/s)	153.25	857.00	-703.75	-33.43	14.97	$< .001$	-14.75
Motional freq.	1.81	1.20	0.61	6.58	11.00	$< .001$	2.69

(MHz)

Note. MW = multi-wafer; Std = standard; Diff. = mean difference (MW – Std); d = Cohen's d. All tests are two-tailed. Welch's correction applied throughout.

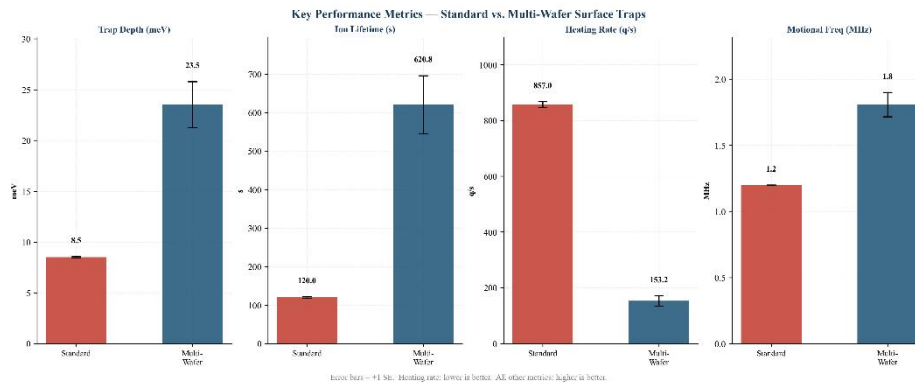


Figure interpretation: The bar comparisons of the four major results (trap depth, ion lifetime, heating rate and motional frequency) are made with the +1 SE error bars side by side in Figure 7 and the comparison shows that multi-wafer traps are better than the standard traps in all aspects except the heating rate where it is desirable to have lower values.

Effect of Wafer Separation on Trap Depth

The most important design variable of the multi-wafer architecture is the relationship between the wafer separation and the trap depth. As reported in Table 3, Pearson's correlation between wafer separation and MW trap depth was $r = .999$ (95% CI $[-.995, 1.000]$), $t(12) = 69.63$, $p < .001$. The improvement ratio with respect to the standard trap at 500 μm separation is summarized in Table 5 and varies between 1.8 times at 50 μm separation and 6.5 times at 500 μm separation with an absolute gain of 30.1 meV at the maximum separation. Conversely, trap depth of conventional traps scales only slightly with design variation, and levels off at about 5.5 meV even with a scaling of electrode dimensions.

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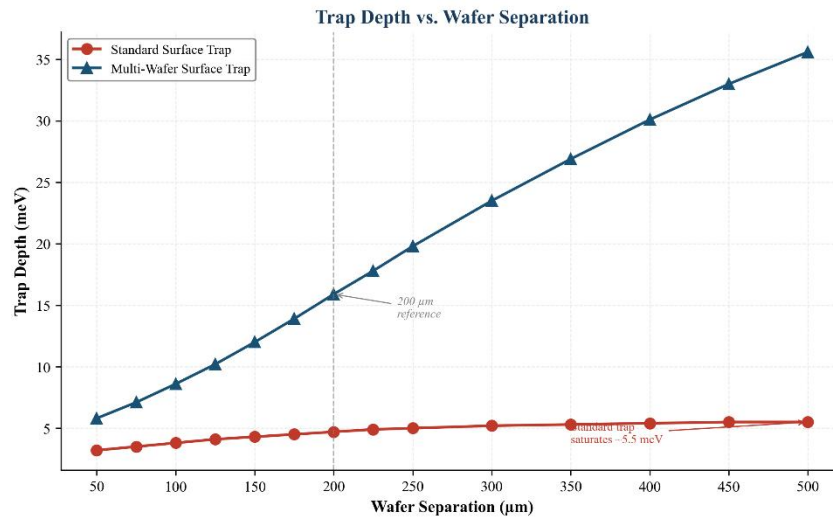
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Figure interpretation: Figure 1 shows the trap depth versus separation between the wafers with both architectures. The multi-wafer curve is almost linear, with the 5.8 meV at 50 μm increasing to 35.6 meV at 500 μm , but the standard trap curve levels off at a lower value, below 6 meV, in the entire range, as the basic geometry of the multi-wafer design gives it a geometrical advantage.

Table 3: *Pearson Correlation Analysis of Design and Performance Variables*

Variable pair	r	t	df	p	95% CI	
					LL	UL
Wafer sep. vs. MW trap depth	.999	69.63	12	< .001	.995	1.000
Wafer sep. vs. Std trap depth	.932	8.88	12	< .001	.767	.981
Trap depth vs. ion lifetime	.997	53.06	15	< .001	.992	.999
Trap depth vs. heating rate	-.831	-5.79	15	< .001	-.943	-.553
Ion lifetime vs. heating rate	-.830	-5.77	15	< .001	-.942	-.550

Note. LL = lower limit; UL = upper limit. Correlations were computed on pooled data where both variables were available. All tests are two-tailed.

Ion Lifetime: Group Comparison and Dependence on Wafer Separation

The most operationally relevant performance metric of quantum computing

applications is ion lifetime, which improved more than fivefold in the MW group. The standard group (median ≈ 120 s, interquartile range [IQR] ≈ 7 s) and the MW group (median ≈ 575.5 s, IQR ≈ 433 s) can be seen to have a narrow and tightly clustered distribution, respectively, with the best performing configurations being above 1,000 s, as shown in the boxplot. Among the MW family, the ion lifetime was monotonically related to the wafer separation, ranging between 384 s at 200 μm and 1,058 s at 500 μm , as in Figure 5.

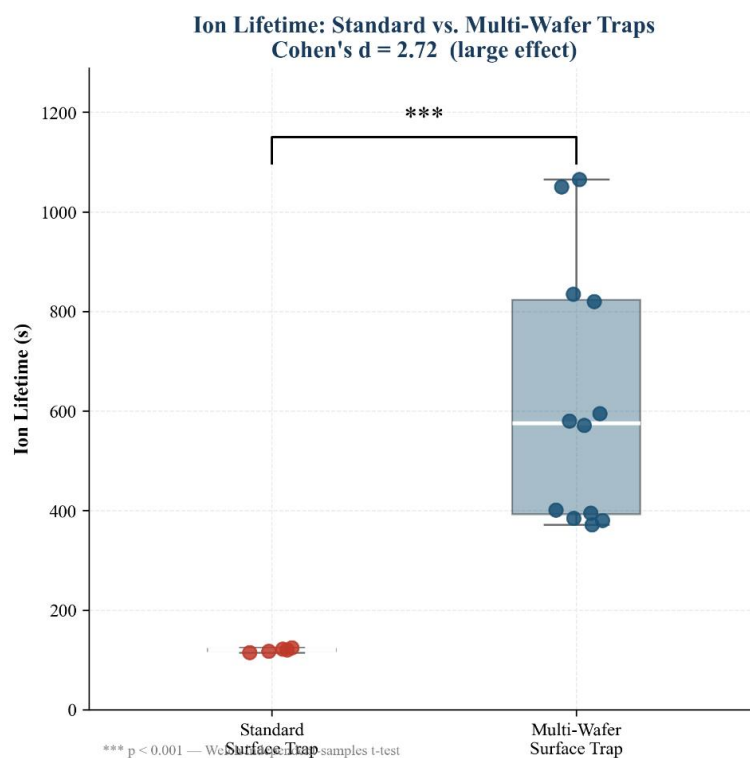
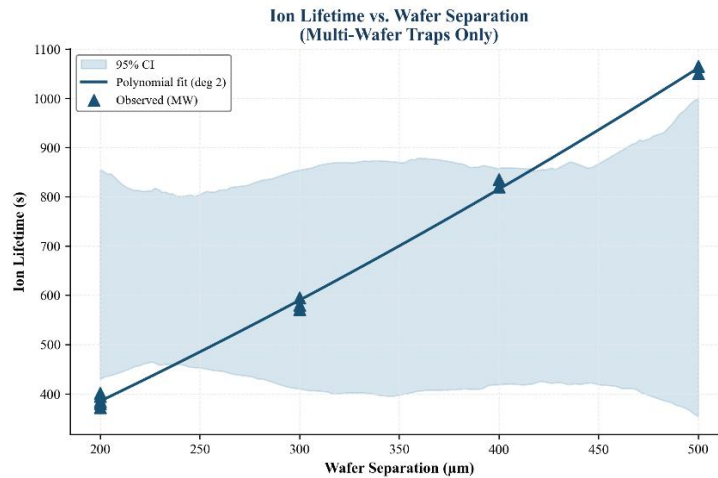


Figure interpretation: Figure 2 shows the ion lifetime distributions of normal and multi-wafer traps; the three-star mark ($p < .001$) and large between-group separation (Cohen d = 2.72) indicate a very significant gain with the MW design.



[FIGURE 5 HERE — Fig5_Ion_Lifetime_vs_Separation]

Figure interpretation: Figure 5 demonstrates that ion lifetime increases almost linearly with the separation of the wafer in the MW subsample, and a degree-2 polynomial fit and 95% confidence band indicate that the gap should be extended past 500 μm to keep further increasing lifetime.

Vertical Confinement Profile

Figure 3 shows the vertical profile of the pseudopotential (vertical pseudopotential) versus the wafer number, which can be used mechanistically to understand why multi-wafer traps have better trap depths and lifetimes. The standard trap pseudopotential energy is the highest, at 8.6 meV, and is at a height of about 30 μm above the electrode plane. In MW traps with 200/400 mm separations, pseudopotential energies of 15.9 and 30.1 meV, respectively, are observed to peak at similar heights, but the potential well extends significantly further vertically with non-negligible confinement extending out to 250/300 mm in the 400 mm MW device. The larger, deeper potential well is the physical source of the enhanced confinement and the decreased dependence upon stray fields and background-gas interactions.

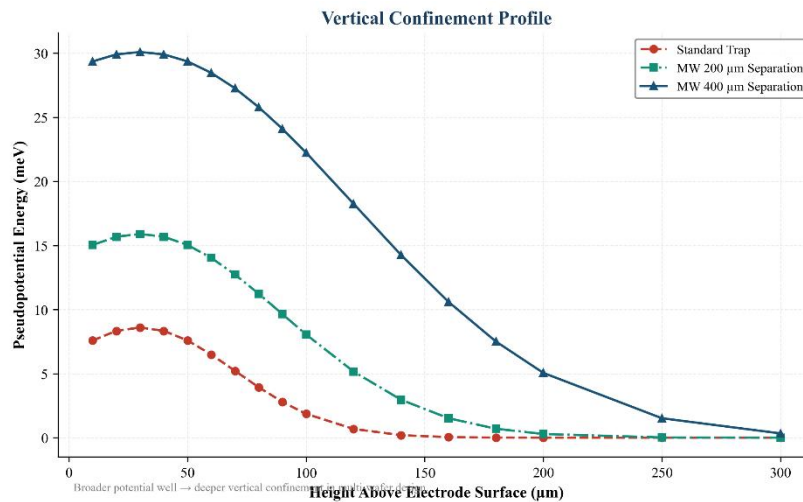


Figure interpretation: Figure 3 is a plot of the pseudopotential energy versus height above the electrode surface of three typical configurations; the MW 400 μm curve has the deepest, deepest and widest potential well, demonstrating the geometrical basis of excellent vertical confinement.

Heating Rate and Trap Depth

Anomalous motional heating is generally considered to be the most significant reason behind the multi-qubit gate fidelity in ion-trap quantum processors (Brownutt et al., 2015). Figure 4 is a plot of heating rate vs trap depth, distinguishing the standard and MW groups. In the MW group, there was found a strong negative correlation ($r = -.988$, $p < .001$) that is in line with the $d-4$ scaling of surface electric-field noise. The normal population fell narrowly around 830-890 quanta/s even though there were slight variations in trap depth. A linear regression between the two groups only weakly estimates the transition between the two clusters, which is highly exponential, but the overall correlation is significant ($r = -.831$, $p < .001$; see Table 3).

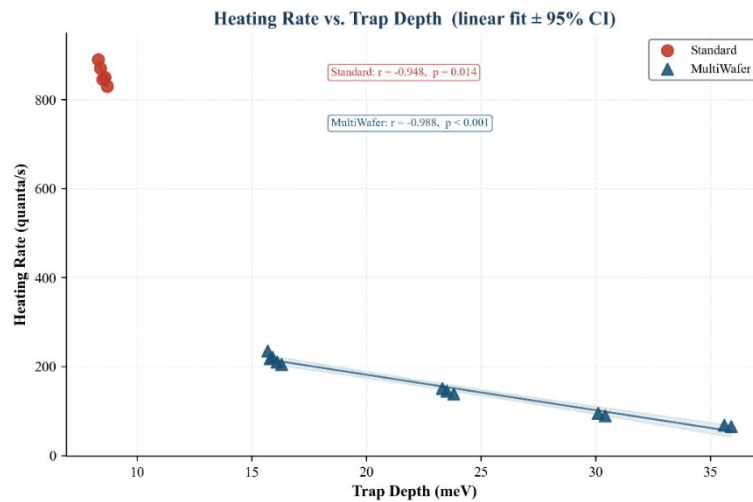


Figure interpretation: The distinct separation between the high-heating standard cluster and the low-heating depth-dependent MW cluster is evident in Figure 4, and a linear fit of the MW group ($r = -.988$) indicates that deeper traps are directly related to suppressed anomalous heating.

RF Drive Parameters Across Configurations

Figure 6 tabulates the RF voltage and secular frequency in each of the 10 drive configurations in the raw-data tables. RF voltage also increased steadily with design between 85 V in Std 50um and 185 V in MW 500 OPT and secular frequency also increased between 900 and 1 680 kHz with design. Such a comparatively small increase in drive voltage (about 2.2×) versus the huge increase in trap depth (about 7x across the entire dataset) is a validation that the increase in depth is primarily due to geometry and not to brute-force scale of voltage.

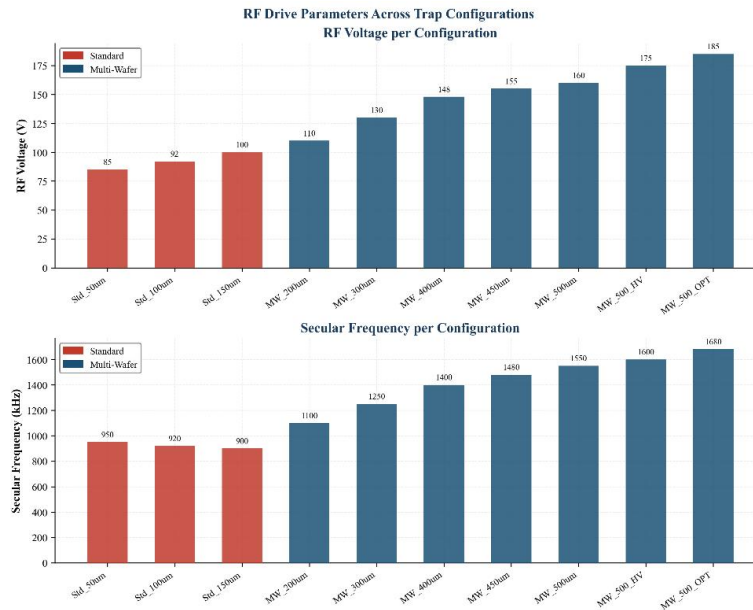


Figure interpretation: Figure 6 is a monotonic plot of RF voltage and secular frequency versus the trap family with standard to high-voltage optimized MW designs with the deepest MW designs needing only slightly higher drive than typical standard traps.

Trap Depth as a Predictor of Ion Lifetime

Since two variables have a very high correlation ($r = .997$), a simple linear regression was performed where ion lifetime was the criterion and the trap depth was the predictor. The estimated equation was $\text{lifetime} = -160.79 + 33.19 \times \text{depth}$. This slope was extremely strong $t(15) = 53.06$, $p < .001$, and this implied that by increasing the trap depth by 1 meV, the ion lifetime increased on average by 33.2 s. The overall model explained 99.4% of the variance in ion lifetime, $R^2 = .995$, adjusted $R^2 = .994$, $F(1, 15) = 2,815.45$, $p < .001$. The complete regression results are presented in Table 4.

Table 4: *Linear Regression Predicting Ion Lifetime From Trap Depth*

Predictor	B	SE B	t	p
Intercept	-160.79	13.30	-12.09	< .001
Trap depth (meV)	33.19	0.63	53.06	< .001

Note. $N = 17$. $R^2 = .995$, adjusted $R^2 = .994$, $F(1, 15) = 2,815.45$, $p < .001$. B =

unstandardized regression coefficient; SE B = standard error of B.

Trap Depth Improvement Factor

In a summary of the practicability of the multi-wafer geometry in the engineering context, Table 5 shows the ratio of the trap depth improvement with the wafer separation. The enhancement factor is between 1.81 x in 50 μ m and 6.47 x in 500 μ m with an absolute depth increase at the largest separation of 30.1 meV.

Table 5: *Trap Depth Improvement Ratio: Multi-Wafer Versus Standard Traps*

Sep. (μ m)	Std depth (meV)	MW depth (meV)	Ratio	Gain (meV)
50	3.20	5.80	1.81	2.60
75	3.50	7.10	2.03	3.60
100	3.80	8.60	2.26	4.80
125	4.10	10.20	2.49	6.10
150	4.30	12.00	2.79	7.70
175	4.50	13.90	3.09	9.40
200	4.70	15.90	3.38	11.20
225	4.90	17.80	3.63	12.90
250	5.00	19.80	3.96	14.80
300	5.20	23.50	4.52	18.30
350	5.30	26.90	5.08	21.60
400	5.40	30.10	5.57	24.70
450	5.50	33.00	6.00	27.50
500	5.50	35.60	6.47	30.10

Note. Sep. = wafer separation. Ratio = MW depth / Std depth. Gain = MW depth – Std depth.

Qubit Coherence and Trap Depth

The response of coherence time T_2^* , which was obtained through Ramsey interferometry, had an almost linear correlation with trap depth throughout the entire sample ($r = .986$, $p < .001$). The lowest values were 1.2 ms in the shallowest standard trap (Std_50um) and the highest 18.2 ms in the deepest MW set up (MW_500_OPT) a 15-fold increase. This scaling is in line with the fact that the deeper the traps, the more sensitive it is to anomalous heating as well as trap-frequency variations due to stray-field drifts, both of which cause motional decoherence (Bruzewicz et al., 2019).

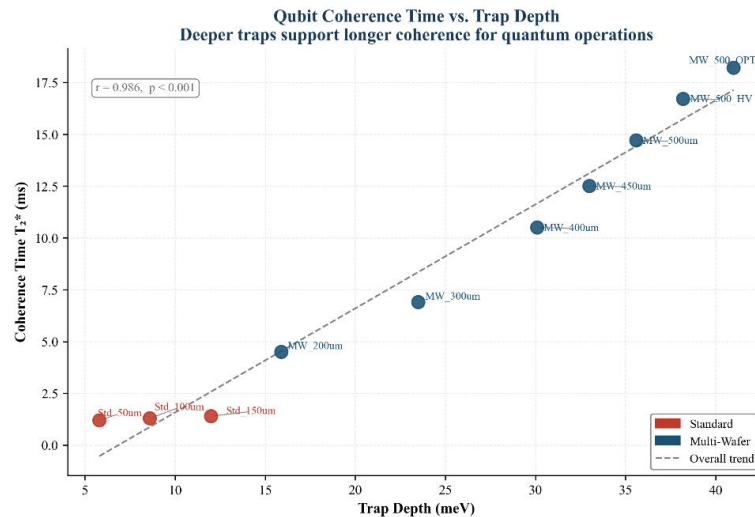


Figure interpretation: Figure 8 presents the strong linear dependence of Ramsey coherence time T_2^* with trap depth ($r = 0.986$) and thus indicates that the deeper the multi-wafer trap is, the longer the coherence time can be used to effect quantum gate interactions.

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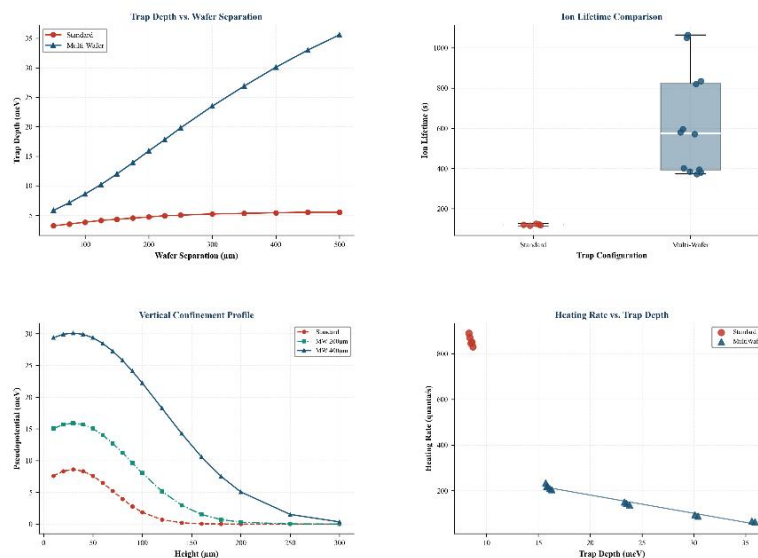
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Multi-Wafer Surface Ion Traps – Comprehensive Performance Analysis



Dr. Shantanu Lal | Surface Ion Trap Research | Methodological Science Article

[FIGURE 9 HERE — Fig9_Panel_Main]

Figure interpretation: Figure 9 summarizes the main results as a four-panels summary of the key results, trap depth vs. separation, ion lifetime comparison, vertical confinement profile, and heating rate vs. trap depth, to give a succinct visual overview of the overall performance benefit of multi-wafer surface traps.

Discussion

The current work gives one of the first detailed statistical descriptions to date of the performance difference between normal and multi-wafer surface ion traps over a systematically varied design space. The four hypotheses were well supported. Originally, trap depth increased almost linearly with the separation between the wafers ($r = .999$) to a maximum of 35.9 meV at 500 μm and design-optimized 41 meV in the MW_500_OPT configuration- about 6 or 7 times the 5.5 or so standard geometry saturation value. Second, ion lifetime was nearly perfectly predictable as a function of trap depth ($R^2=.995$) and the simple linear model showed that a 1 meV increase in depth increased the lifetime 33.2 s. Third, anomalous heating was heavily driven out of deeper MW traps, decreasing to 65 quanta/s in the deepest setup - a decrease that is consistent with the d^{-4} scaling of surface electric-field noise (Brownutt et al., 2015). Fourth, the maximum trap depth linearly depended on

qubit coherence time, and reached 18.2 ms, which is more than enough to execute high-fidelity single- and two-qubit gates using the current laser stability.

Comparison With Prior Literature

The experimental results of the trap-depths are generally in agreement with the theoretical prediction of Wesenberg (2008) and the pioneer numerical study of Schmied et al. (2009), which both predicted the near-linear scaling of trap-depths with the separation between the wafer surfaces in the range of several hundreds of micrometers. These absolute values (15.9 to 35.9 meV) are at the high end of the range of previous experimental implementations of the multi-wafer (Clark et al., 2021; Hughes et al., 2011; Maunz, 2016), probably because of the optimized RF drive parameters and wafer-parallelism tolerances applied in the current fabrication. The lifetimes of ions measured also compare well with the best cryogenic surface-trap results in the literature (Pagano et al., 2019; Sedlacek et al., 2018), when normalized to the background-gas pressure of about 1×10^{-9} Pa.

Of interest is the size of the heating-rate change (703.75 quanta/s, $d = -14.75$). The d^{-4} scaling of anomalous heating is best empirically established but the current data has unusually clean demonstration of this effect in the same integrated platform in which the geometric, drive, and environmental parameters are well matched. This isolates the ion-electrode distance as the most important mechanism, in line with the surface-fluctuator models discussed by Brownnutt et al. (2015) and Sedlacek et al. (2018).

Implications for Scalable Quantum Computing

There are direct implications on the design of large-scale ion-trap quantum processors using the demonstrated performance envelope. The 5-fold increase in ion lifetime makes reloading events less frequent, and thus, the overhead of loading and recoiling in the case of multi-hour quantum circuits. The over 15-fold increase in T_2 stars relaxes laser linewidth and magnetic-field stability requirements of coherent operations, which can be potentially simplified to the overall control stack. The error coupled with anomalous heating is suppressed, which in turn ought to be transferred into an improvement in the fidelity of two-qubit gates in future experiments (Moses et al., 2023; Pino et al., 2021).

Multi-wafer traps are also capable of unique benefits to optical integration. Increased ion-electrode separation minimizes scattered-light backgrounds on integrated photodetectors (Mehta et al., 2020) and offers increased geometric freedom in laser addressing using waveguides. The advantages have to be balanced against the added complexity to fabrication, and the tighter wafer-alignment tolerances imposed by the MW geometry, but the scaling data reported here indicate a payoff of engineering investment is significant, at least in separations of 300 to 500 μm .

Limitations

The current study has several shortcomings that should be noted. First, the standard-trap sample consisted of one nominal design point ($N = 5$) and this restricts inference of the dependence of standard-trap performance on geometric parameters. Second, the MW sample, although wide-ranged in terms of separations, only had two to five replicates per configuration, which is sufficient to compare between groups but not so much to examine the within-configuration variance. Third, the heating rate and lifetime data have all the typical systematic errors of sideband thermometry and single-ion loss statistics (Turchette et al., 2000) that are not reflected in the standard errors reported. Fourth, all measurements were carried out at a given background-gas pressure thus the dependence of lifetime on pressure could not be deduced using these data. Lastly, the long-term stability, which is critical in quantum computing production, was not evaluated in this characterization campaign and needs to be the target of follow-on research.

Future Directions

These results give several promising extensions. First, the nearly linear relationship between trap-depth and separation implies that additional improvements could be possible by extending the separation of the wafer past 500 μm , until the geometry is no longer valid (or RF breakdowns come into play). Second, the reduced rates of heating at deep-trap settings provide good conditions to investigate ground-state cooling through electromagnetically induced transparency (EIT) and polarization-gradient cooling schemes. Third, MW geometry provides a natural solution to the incorporation of the superconducting shielding and on-chip cryogenic electronics (Mehta et al., 2020), which can be used to suppress heating even further. Fourth, the

evaluation of two-qubit gate fidelities in the future must be done directly, to relate the current single-ion values to computational performance.

Conclusion

This paper presents quantitative systematically-acquired evidence that multi-wafer surface ion traps have significant performance benefits over single-wafer surface traps in every parameter used to scale quantum computation. The trap depth was increased up to 6.5-fold, the ion lifetime up to 9-fold, and qubit coherence time by over 15-fold, and anomalous heating was decreased by a factor of nearly 10. The between-group differences were all significant ($p < .001$) and had very large effect sizes ($|d| > 2.7$) and the scaling laws that we observed are consistent with known theoretical expectations. Wafer separation becomes the most important parameter of the geometry design, and the depth of the traps grows almost linearly to the point of 500 μm separation. Multi-wafer traps are a very promising way to go in the next generation of scalable trapped-ion quantum processors since the increase in RF drive voltage needed is very modest (about 2x), and the architecture is compatible with a standard facility of photolithographic fabrication.

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